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Docket No. BU9-98-225DIV

**AMENDMENTS TO THE CLAIMS:**

**Please cancel claim 41 without prejudice or disclaimer.**

1-7. (Canceled)

8. (Currently amended) A semiconductor substrate comprising:

a trench region comprising at least one trench, said trench comprising a single layer of high-density plasma (HDP) oxide having an unpolished upper surface; and

a non-trench region having an upper surface which is substantially co-planar with said unpolished upper surface of said single layer of said HDP oxide, said upper surface of said non-trench region comprising implanted dopants,

wherein said upper surface of said HDP oxide comprises a slightly-etched surface, such that a thickness of said single layer of HDP oxide comprises an originally-deposited thickness of said oxide less an amount of said oxide removed by a slight etch ~~a substantially as-deposited thickness.~~

9-14. (Canceled)

15. (Currently amended) A semiconductor substrate comprising:

a trench region comprising a plurality of trenches, each of said trenches comprising a single layer of high density plasma (HDP) oxide having an unpolished upper surface; and

a non-trench region having an upper surface which is substantially co-planar with said unpolished upper surface of said single layer of said seamless HDP oxide, said upper surface of said non-trench region comprising implanted dopants,

wherein said upper surface of said HDP oxide comprises a slightly-etched surface, such that a thickness of said single layer of HDP oxide comprises an originally-deposited thickness of said oxide less an amount of said oxide removed by a slight etch ~~a substantially as-deposited~~

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thickness.

16-22. (Canceled)

23. (Currently amended) A semiconductor substrate comprising:

a trench region comprising at least one wide trench and at least one narrow trench, each of said trenches comprising a single layer of high density plasma (HDP) oxide having an unpolished upper surface; and

a non-trench region having an upper surface which is substantially co-planar with said unpolished upper surface of said single layer of said seamless HDP oxide, said upper surface of said non-trench region comprising implanted dopants,

wherein said upper surface of said HDP oxide comprises a slightly-etched surface, such that a thickness of said single layer of HDP oxide comprises an originally-deposited thickness of said oxide less an amount of said oxide removed by a slight etch ~~a substantially as-deposited thickness.~~

24. (Previously presented) The semiconductor substrate according to claim 8, wherein said high density plasma oxide comprises non-conformal high density plasma oxide.

25. (Previously presented) The semiconductor substrate according to claim 8, wherein said at least one trench comprises at least one wide trench and at least one narrow trench.

26. (Previously presented) The semiconductor substrate according to claim 8, wherein said high density plasma oxide comprises fluorine-doped high density plasma oxide.

27. (Previously presented) The semiconductor substrate according to claim 8, wherein said high density plasma oxide comprises silicon dioxide.

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28. (Previously presented) The semiconductor substrate according to claim 24, wherein said high density plasma oxide comprises silicon dioxide doped with fluorine.
29. (Previously presented) The semiconductor substrate according to claim 8, wherein said surface of said filler material and said surface of said substrate are planarized without reactive ion etching.
30. (Currently amended) The semiconductor substrate according to claim 8, wherein said at least one trench comprises a shallow trench isolation ~~isolations~~.
31. (Previously presented) The semiconductor substrate according to claim 8, wherein said upper surface of said single layer of HDP oxide and said upper surface of said non-trench region are planarized without chemical mechanical polishing.
32. (Previously presented) The semiconductor substrate according to claim 8, wherein said upper surface of said single layer of HDP oxide is substantially scratch-free.
33. (Canceled)
34. (Previously presented) The semiconductor substrate according to claim 8, further comprising:  
a thin oxide layer grown on said upper surface of said substrate.
35. (Previously presented) The semiconductor substrate according to claim 8, wherein said upper surface of said single layer of HDP oxide is free of chatter marks.
36. (Previously presented) The semiconductor substrate according to claim 23, wherein

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said at least one wide trench is formed adjacent to said at least one narrow trench.

37. (Previously presented) The semiconductor substrate according to claim 23, wherein said HDP oxide comprises fluorine-doped HDP oxide.

38. (Previously presented) The semiconductor substrate according to claim 23, wherein said high density plasma (HDP) oxide comprises non-conformal HDP oxide.

39. (Previously presented) The semiconductor substrate according to claim 37, further comprising:

a thin oxide layer grown on said upper surface of said substrate, said thin oxide layer comprises a high-purity oxide.

40-41. (Canceled)

42. (Previously presented) The semiconductor substrate according to claim 8, wherein said unpolished upper surface of said HDP oxide has been etched to expose a pad layer formed on said upper surface of said non-trench region.

43. (Previously presented) The semiconductor substrate according to claim 8, wherein said HDP oxide comprises a phosphorus-doped oxide.

44. (Previously presented) The semiconductor substrate according to claim 8, wherein said HDP oxide comprises a boron-doped oxide.

45. (Previously presented) The semiconductor substrate according to claim 8, wherein an entirety of said upper surface of said HDP oxide comprises said slightly-etched surface.

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46. (Previously presented) The semiconductor substrate according to claim 8, wherein said slightly-etched surface comprises an isotropically-etched surface.